Maskless and Resistless MOSFET Fabrication using Ion Beam Lithography*

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The manufacture of CMOS integrated circuits will eventually require techniques for patterning sub-10nm features, with sub-25 nm half-pitch.[1] Mask costs for deep-UV (eventually EUV) lithography will continue to escalate with each new generation of technology, and will even become prohibitive for low-volume IC products. Concurrently, new resists must continually be developed to provide optimal resolution with adequate line-width control and throughput, as ever shorter wavelengths of light are used. In order to circumvent these issues, maskless and resistless patterning techniques are desirable. Focused ion beams have already been used for maskless patterning of sub-10nm features in resist[2] and can be directly (without resist) used to form oxide selectively on the surface of Si. To achieve reasonable exposure throughput, a high-brightness multi-cusp plasma source can be used together with an array of independently controlled ion-beam columns.[3] In this work, we demonstrate that it is possible to fabricate a MOSFET entirely without any masks or resist, by using ion beam lithography. This approach can greatly simplify the manufacture of nanoscale integrated circuits in the future.

The multi-cusp plasma source is capable of producing a variety of ion species (such as O_2^+, BF_2^+, P^+)[4] and it can achieve relatively high brightness (440A/cm^{2}Sr was recently demonstrated)[3]. An all-electrostatic, two-lens column (Fig. 1) is used to extract the ion beam from the source and focus it on the target. The demagnification factor is ~10×; however, the beam spot size at the target is ~16 μm for an extraction aperture of 50 μm, due to aberrations.

Silicon can be selectively oxidized by low-energy oxygen ions. The process for direct patterning of a poly-Si film is illustrated in Fig. 2(a). O_2^+ ions are selectively implanted with energy 3 keV, to form a thin silicon dioxide layer on the surface, which serves as a hard mask in a subsequent reactive-ion etch process used to pattern the poly-Si film. No deflector was included in the focusing column, so patterns of SiO_2 were formed simply by mechanically moving the wafer holder. Fig. 2(b) and 2(c) show a patterned poly-Si line (140 nm thick) and its profile, respectively. The scan rate of the sample stage was 100 μm/sec, so that the oxygen dose was ~10^{15} cm^{-2}. The width of the patterned poly-Si is ~11 μm, which matches simulation (Munro code) results reasonably well.

The SOI MOSFET fabrication process is shown in Fig. 3. First, the Si is thinned down to ~30 nm by thermal oxidation. The active areas are then directly patterned using a focused oxygen ion beam at a dose of ~10^{14} cm^{-2} followed by an HBr-based reactive ion etch (RIE). Afterwards, 8 nm gate oxide is thermally grown (900¡C, 12 minutes), and 120 nm of *in-situ* phosphorus doped poly-Si film is deposited. The poly-Si is then patterned using the focused oxygen ion beam followed by RIE. A focused beam of phosphorus ions is used to dope the source and drain (S/D) regions. Finally, rapid thermal annealing is performed to activate the implanted dopants, and a dilute HF solution is used to remove oxide from the surfaces of the S/D regions, to allow for direct probing. A completed MOSFET is shown in Fig. 4. Electrical characterization of the fabricated transistors is in progress, and results will be reported at the conference.

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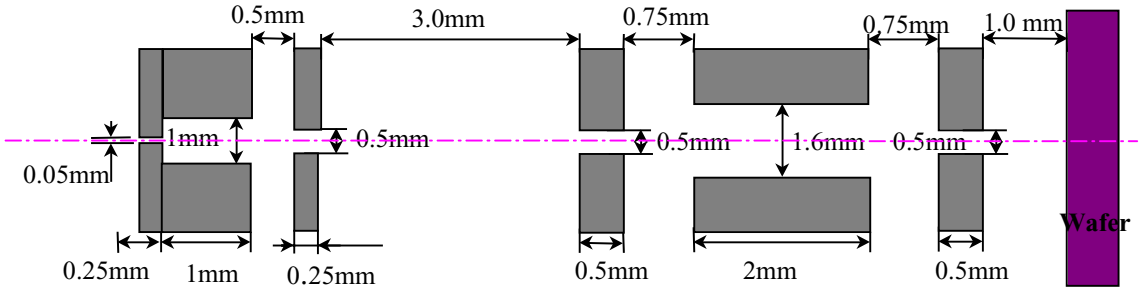

Figure 1: Schematic diagram of the two-lens column used in this work.

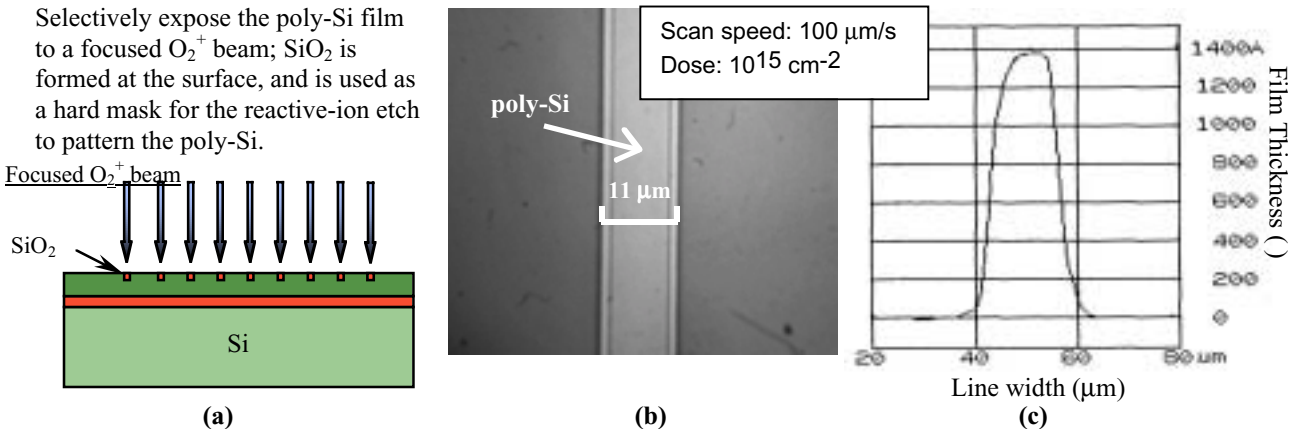

Figure 2: (a) Process for direct patterning of poly-Si **(b)** Micrograph of poly-Si line patterned with a focused O_2^+ beam at a dose of 10^{15}cm^{-2} **(c)** Profile map of the poly-Si line.

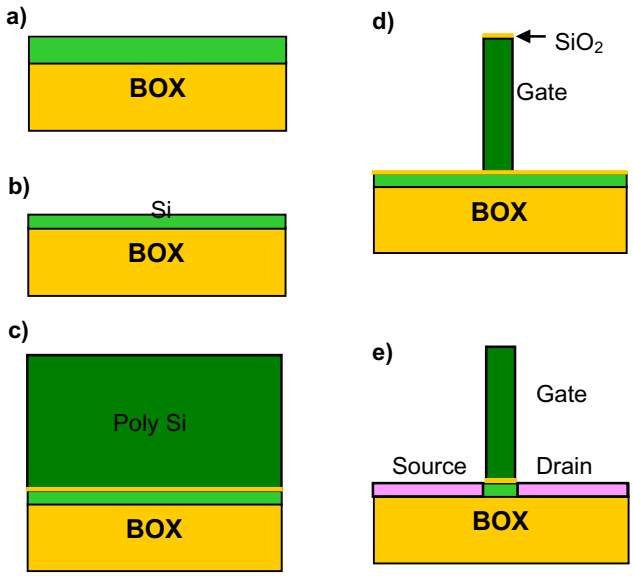

Figure 3: SOI MOSFET fabrication process. **a)** SOI starting substrate (100 nm Si on 400 nm buried oxide); **b)** thin the Si by thermal oxidation, then pattern the active regions using a focused O_2^+ beam followed by reactive ion etching; **c)** grow the gate oxide and deposit *in-situ* doped poly-Si; **d)** pattern the poly-Si using a focused O_2^+ beam followed by RIE; **e)** selectively dope the source and drain regions using a focused P^+ beam, then activate the dopants with a rapid thermal anneal. Remove oxide over S/D regions prior to probing.

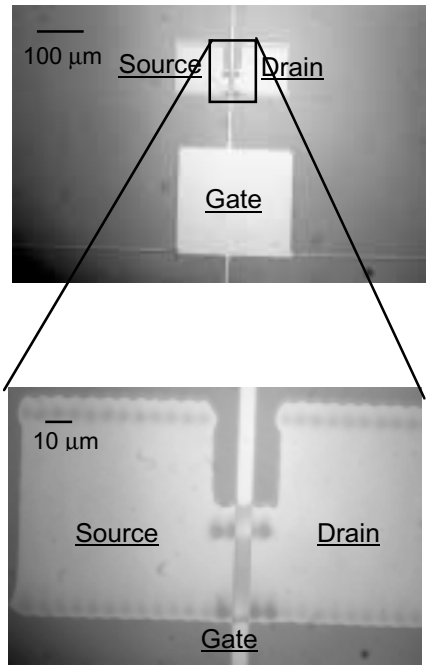

Figure 4: Micrographs of SOI MOSFET fabricated without any masks or resist.